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Analysis and Design of a Low Voltage Si LDMOS Transistor

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ABSTRACT : This paper presents a compact model of lateral double diffused MOS (LDMOS) transistor having small size and got good result with different characteristics. This model is designed with ATLAS SILVACO and get better simulations of breakdown voltage, on resistance etc. comparing with reference LDMOS. We have designed this device with channel 0.3 µm length and gate 0.75 µm length.
KEYWORDS - ATLAS, Breakdown Voltage, Capacitance, LDMOS, On Resistance.

I. INTRODUCTION

Lateral double diffused MOS (LDMOS) transistors are mostly used in high voltage and RF applications. These applications include high breakdown voltage, low on resistance and compatibility with standard CMOS and BiCMOS manufacturing process. Comparing with other semiconductor devices, an accurate and physical compact model is critical for LDMOS based circuit design because size of this device is so large. That's the reason LDMOS device are seldom used compared with other semiconductor devices. Today, the size of LDMOS device is needed to smaller and smaller for safe operations [2].Presence of the lightly doped drift region in LDMOS device has different characteristics effect on breakdown voltage w.r.t conventional MOSFET. Impact ionization in LDMOS, which depends on the bias conditions, primarily occurs either in the intrinsic MOSFET or in the drift region. The purpose of this paper is to provide a new resize device with better simulated characteristic results [1]-[4].

II. DEVICE STRUCTURE AND SIMULATIONS

The schematic cross section of the reference and proposed LDMOS device is illustrated in Fig.1 and fig. 2. The LDMOS parameters used in our simulation are shown in Table 1. All the device parameters of the new structure are equivalent to those of the reference LDMOS [5].

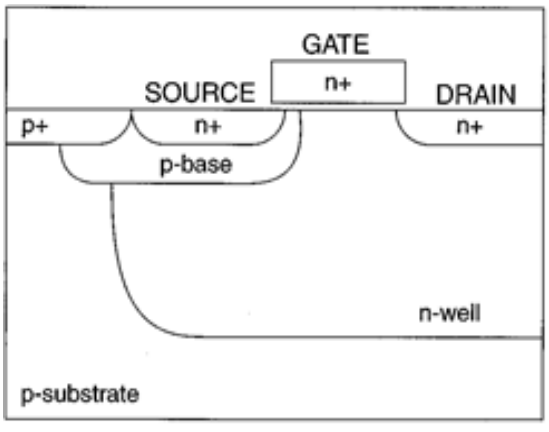


Fig.1: LDMOS Cross Section [5]

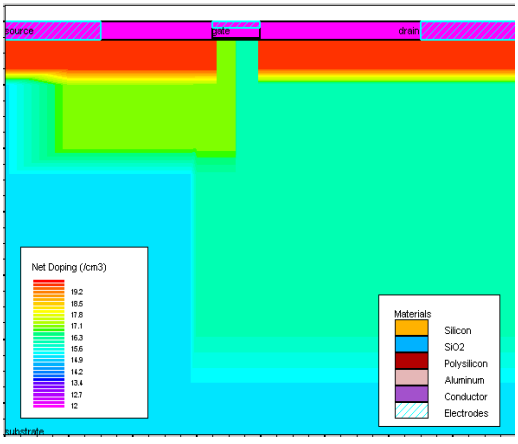


Fig.2: Simulator based LDMOS model

TABLE 1: SIMULATION PARAMETERS

Parameters	Value
Gate length	0.75 µm
Channel length	0.3 µm
Oxide thickness	35 nm
Thickness of n well	5 µm
Thickness of p body	1 µm
Doping	
Substrate (p type)	10^{15} cm^{-3}
Source & drain diffusion	$5e^{19}$ cm^{-3}
P body doping	10^{17} cm^{-3}
N well doping	10^{16} cm^{-3}

Two dimensional numerical simulations of the proposed structure are done with ATLAS simulator. In addition to, Poisson and drift/diffusion equations, SRH (Shockley-Read- Hall) and Auger models are considered for generation/recombination and also IMPACT SELB for impact ionization. These simulations methods allow taking into account carrier velocity saturation, carrier–carrier scattering in the high doping concentration, dependence of mobility on temperature and vertical electric influence. Breakdown mechanism is investigated by both two dimensional process simulations with SILVACO [6]-[9]. It is worth noting that the two dimensional (2D) simulator is calibrated to experimental data.

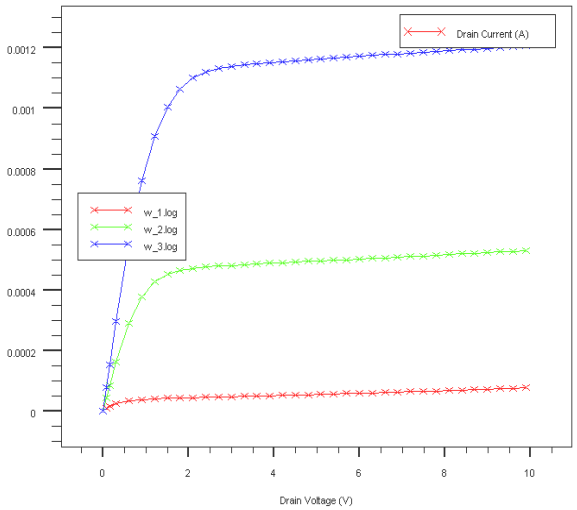
III. RESULTS & DISCUSSION

A. Drain Characteristics

The drain characteristics for the LDMOS structure with an LDD dose of 1×10^{16} cm^{-3} are shown in fig.3 for gate bias voltages ranging from 1 to 10V. It can be seen that the output resistance decrease at high drain voltages due to the onset of impact ionization which is shown in fig.6 and fig.8. The non-linear increase in drain current is due to the channel length modulation.

B. Transfer Characteristics

Transfer characteristics shows the relation of the drain current (I_D) with the variation of the gate voltage (V_{GS}) keeping the drain voltage (V_{DS}) fixed. The drain-current flows only if the gate voltage exceeds the threshold voltage V_T. However, for LDMOS after the threshold voltage the current of LDMOS is lower than that of conventional MOS. This is due to the fact that it has higher on-resistance. Ron is higher due to the addition of the drift region. At V_{DS}=0.1 Volt and 0.2 Volt, the drain current is plotted against gate voltage (V_{GS}) are shown in fig.4.



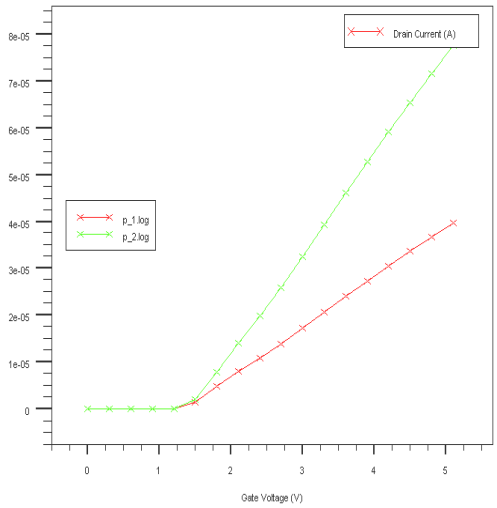


Fig.3. IV characteristics with different gate voltage. Fig.4: I_D vs. V_{GS} plot having threshold Voltage (V_T) = 1.3V.

C. Breakdown Voltage

In MOSFET when VDS exceeds a certain value, the drain current abruptly increases. As V_{DS} increases, the peak electric field at drain end of the channel also increases. When

the peak electric field approaches the middle of 10^5 V/cm range, the impact ionization takes place at the drain junction leading to sharp increase in I_D. The high-energy electrons, which have gained energy from electric field, have sufficient kinetic energy to generate secondary electrons and holes by impact ionization. The generated electrons are collected at the drain and then added to I_D, while the holes flow to the substrate contact resulting in substrate current. In LDMOS the drift region supports the applied voltage and protects the channel region from high voltage. At the applied potential, the depletion stretches along the lateral length or surface over a much longer distance. Therefore, the electric field is far below the critical field (Ec) and hence more voltage can be applied before breakdown occurs. It can also be seen from impact ionization rate in fig.6. That it is shifted from the drain.

In present work, the breakdown occurs at 13.75 V when gate voltage is at 0 V. By increasing gate voltage breakdown voltage decreases. Fig.5. shows the breakdown curves with varying gate voltage in range 0 to 10 V.

D. Impact Ionization

Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. For example, in semiconductors, an electron (or hole) with enough kinetic energy can knock abound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an electron-hole-pair. If this occurs in a region of high electrical field then it can result in avalanche breakdown. In a device the original charge carrier is created by the absorption of a photon [10]-[12]. In some sense, the impact ionization is the reverse process to Auger recombination. For n-channel MOSFET, the impact ionization takes place at the junction of substrate and drain region. As voltage is applied at the drain region, the avalanche breakdown occurs for a very low voltage. However, for LDMOS, the impact ionization occurs at the junction of drift region and substrate, which is away from the drain region (as shown in Fig.5). For this reason, this device shows a higher breakdown-voltage.

The electric field is high at drift region, thus avoiding a premature avalanche before reaching the required breakdown voltage. The potential linearly increase with increase gate voltage shown in fig 7. The high electric

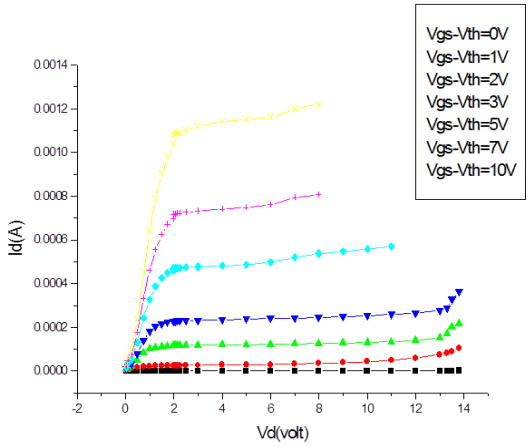


Fig.5: BV vs. V_D at the different gate voltage

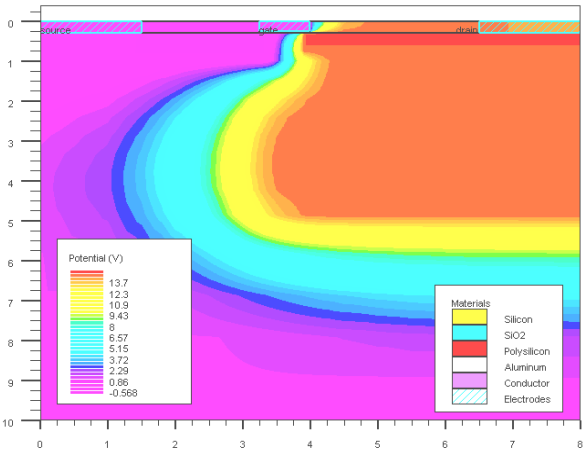
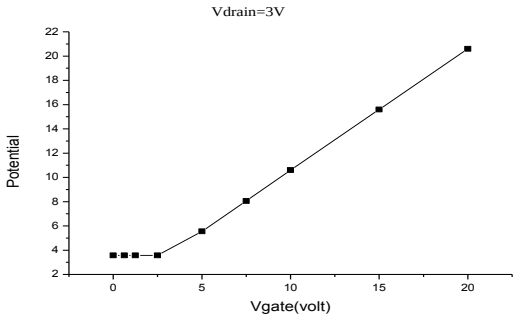


Fig.6: Impact ionization at breakdown.



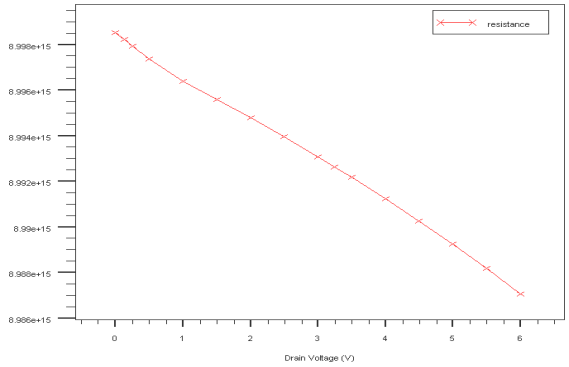


Fig.7: Plot between potential vs. gate voltage. Fig. 8: R_{ON} resistance vs. drain voltage, with increase drain voltage, on resistance decreases.

field peak is located at the drift/drain edge where the high impact ionization rate at this point is responsible for the avalanche mechanism. The high electric field region is found at the body/drift junction, being responsible of the wide P-body depletion and the high increment of the electron current density at the channel region.

E. On Resistance

In LDMOS, drift region represents a dynamically varying resistance for current flow and also introduces additional charges. When drain voltage increases from 0 to 6 volts, drain current increases, resistance decreases.

A. Capacitance and Trans conductance

Other peculiar features are observed in capacitance, showing strong sharp peaks, which significantly change depending on the structure as well as Doping levels. The Trans conductance increases sharply with low gate voltage until 1.6 vaults and then rapidly decreases due to the compression phenomenon and lightly doped drain region.

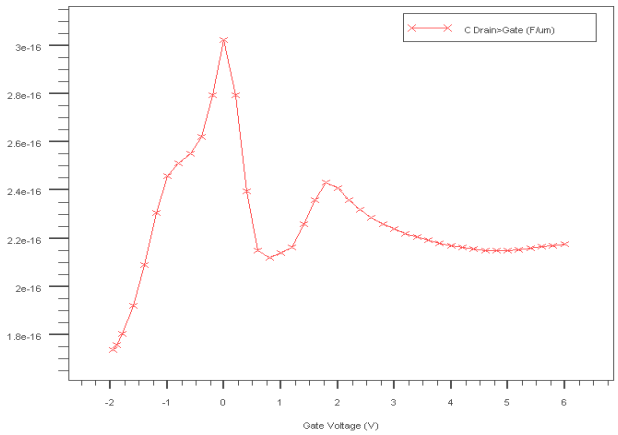


Fig.9: Capacitance vs. gate voltage

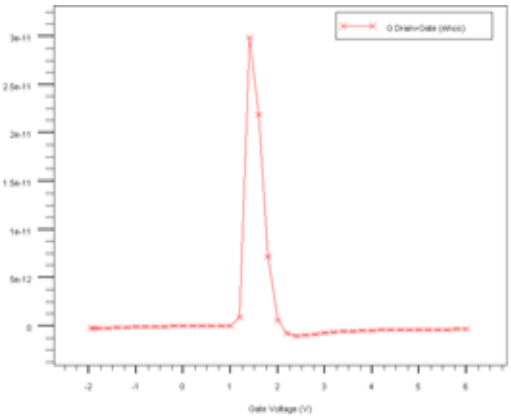


Fig.10: Trans-conductance vs gate voltage.

IV. CONCLUSION

The results of two dimensional numerical simulations have been provided to describe its characteristics. The proposed device gives better result than reference device. The breakdown voltage of this device is higher compared with reference device. The R_{ON} resistance is lower compared with reference device. The feedback capacitance is reduced so breakdown voltage is improved.

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