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A Virtual Ground Based SRAM Cell with NBTI Recovery Boosting

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Abstract: SRAM are the most promising high speed memory elements which are used in most of the Processors and controllers. Although the effect of leakage currents in SRAM memories is a great problem for the future architectures. In this paper we are going to redesign the SRAM for the purpose of more power & area reduction than the existing type of designs as well as the new design which is combined of NBTI Stability Improvement with read Error Reduction Logic and with Process Variation Tolerance Effect is Proposed and it's compared with the existing technologies & the nanometer technology. The simulations were carried out using Tanner EDA Tools. The Simulations are done under TSMC018 technology rules.

Keywords: NBTI Reduction, Recovery Boosting, SRAM Design, Process Variation Tolerance.

Introduction:

RELIABILITY is one of the biggest challenges facing the microprocessor industry today. With continued technology scaling, processors are becoming increasingly susceptible to hard errors. Hard errors are permanent faults that occur due to the wearing out of hardware structures over time. These failures occur partly due to design-time factors such as process parameters and wafer packaging, as well as runtime factors such as the utilization of the hardware resources and the operating temperature. It is important to ensure that the reliability of the microarchitectural structures in the processor is maximized so that one can make use all the available hardware resources effectively over the entire service life of the chip.

As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. As microprocessor speeds increase from 25 MHz to 100 MHz, to 250 MHz and beyond, systems designers have become more creative in their use of cache memory, inter leaving, burst mode and other high-speed methods for accessing memory. The old systems sporting just an on-chip instruction cache, a moderate amount of DRAM and a hard drive have given way to sophisticated designs using multilevel memory architectures. One of the

primary building blocks of the multi-level memory architecture is the data cache. There are many reasons to use an SRAM or a DRAM in a system design. Design tradeoffs include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design.

Speed: The primary advantage of an SRAM over a DRAM is its speed. The fastest DRAMs on the market still require five to ten processor clock cycles to access the first bit of data. Although features such as EDO and Fast Page Mode have improved the speed with which subsequent bits of data can be accessed, bus performance and other limitations mean the processor must wait for data coming from DRAM. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times

equal to the clock cycle used by the microprocessor. With a well-designed cache using ultra-fast SRAMs, conditions in which the processor has to wait for a DRAM access become rare.

Density. Because of the way DRAM and SRAM memory cells are designed, readily available DRAMs have significantly higher densities than the largest SRAMs. Thus, when 64 Mb DRAMs are rolling off the production lines, the largest SRAMs are expected to be only 16 Mb.

Volatility. While SRAM memory cells require more space on the silicon chip, they have other advantages that translate directly into improved performance. Unlike DRAMs, SRAM cells do not need to be refreshed. This means they are available for reading and writing data 100% of the time.

Cost. If cost is the primary factor in a memory design, then DRAMs win hands down. If, on the other hand, performance is a critical factor, then a well-designed SRAM is an effective cost performance solution.

Custom features. Most DRAMs come in only one or two flavors. This keeps the cost down, but doesn't help when you need a particular kind of addressing sequence, or some other custom feature. IBM's SRAMs are tailored, via metal and substrate, for the processor or application that will be using them. Features are connected or disconnected according to the requirements of the user. Likewise, interface levels are selected to match the processor levels. IBM provides processor specific solutions by producing a chip with a standard core design, plus metal mask options to define feature sets.

Even though the SRAM is high Power Consuming Element to remove this unwanted power consumption a new Schmitt trigger based SRAM memory is proposed in our reference Paper. The proposed design is built after analyzing the different types of SRAM using low power design techniques the simulations were done under Tanner EDA Tool.

The Problem Found in the existing SRAM Designs are listed below:

- SRAMs are consuming most of the power of the core Processor Element.
- The leakage in the SRAM circuit is high when compared to the all other processor components.
- As its consuming much power heat dissipation also occurs
- So less efficient than all other elements.

THE SINGLE-ENDED 8T CELL

Due to the stability limitations of 6T SRAM cell at low supply voltages, 8T SRAM is suitable for multimedia applications [9]. The two main advantages of 8T over 6T cell are:

1) As the read path is decoupled from the storage nodes, the cell ratio β becomes unimportant and the pull down transistors can be scaled in size thereby reducing the area overhead.
2) The second advantage comes handy in lowering the power in particular because the read '1' operation in 8T SRAM does not consume any power.

For applications like video encoders etc, where there is a lot of statistical similarity and data correlation, this becomes advantageous as most of the bits stored are '1's by the use of majority logic and data-bit reordering [9]. The 8T SRAM cell has the normal 6T SRAM design with a read decoupled path consisting of two nMOS transistors.

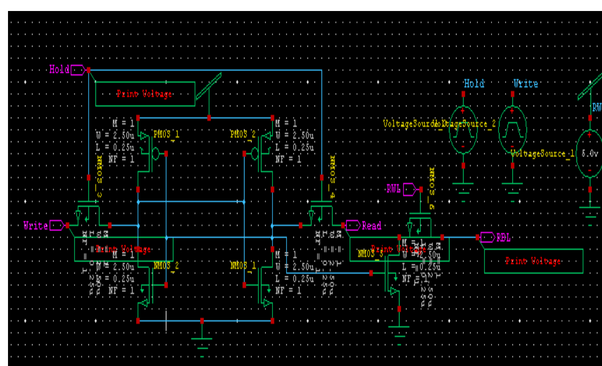

Figure 1: 8T SRAM without Charge Sharing Logic

Read operation of the 8T cell: At the start of the read cycle the read bit line is pre-charged to full swing voltage. After the pre-charge phase is over, Read Word Line (RWL) is asserted that drives the access transistor M5 ON. If the data stored at node Q is '0' the transistor M6 is on and Read Bit Line (RBL) discharges through

the transistors M5 and M6 to ground. This dip in the voltage of the RBL is detected by the sense amplifier attached at the end of the column and it generates a data output value of '1'. During the read '1' operation access transistor M5 is ON but as Q is '1' M6 is OFF. Hence no discharge current flows through the read path. Only a small amount of leakage current flows which is called bit line leakage.

Write operation of the 8T cell: Write operation of the 8T cell is similar to 6T cell but pre-charge circuitry at the bit lines is replaced by a write driver.

10T CELL DESIGN

The architecture of the 10T cell is similar to the single ended 8T cell. In addition to the 8 transistors, 2 transistors are added in the decoupled read path and instead of draining the read current to ground the read path is connected to BL & BLB through these 2 transistors as shown in figure.

B. Analysis Of The Proposed 10T Cell

The proposed cell works on three strategies for the power reduction.

1) Strategy for Read Power Reduction

The main component of read power in 8T cell is the charge /discharge power of read bit line. During the read '0' operation the BL is discharged completely to ground.

Hence, if the swing at the read bit line is somehow reduced, the read power consumption can be reduced. Moreover, the use of sense amplifier makes it possible to detect small voltage swings of up to 50 mV. Hence, a very low discharge of bit line is enough to read a data value '0'. This cell behaves as an automatic bit line swing limiter. The BL and BLB are dedicated bit lines for write operation in 8T cell. During write operation, one of the bit lines BL/BLB remains low and the other remains high. Two different scenarios are possible depending upon the value of the last data written in the column.

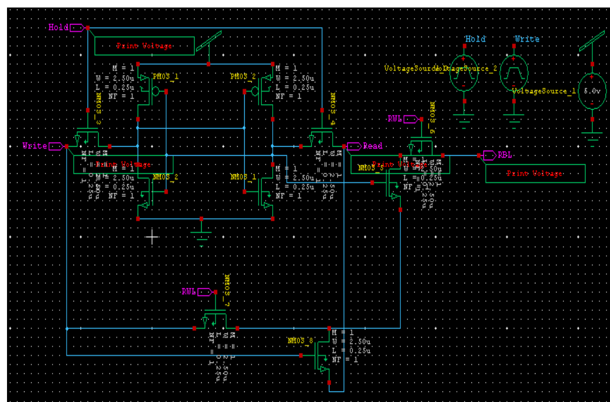

Figure 2: 10T Architecture with Charge Sharing Logic

Scenerio1:- If the last written data was '0', BLB is high and BL is low. If any cell in the column now reads a value '0', the RBL discharge goes though the read path transistors M5, M6 and M7 to BL. As the BL is floating during the read cycle, the charge is shared between the read bit line RBL and bit line BL.

Scenerio2:- If the last written data was '1', BL is high and BLB is low. The high BL enables the transistor M8. If any cell in the column now reads a value '0', the RBL discharge goes though the read path transistors M5, M6 and M8 to BLB.

In both the scenarios the charge is shared between the read bit line RBL and the uncharged bit line BL/ BLB during read '0' operation. In effect, the charge sharing has two advantages. First is that due to sharing of charges, read bit line does not discharge completely and stays at a mid-level voltage. In the next read cycle, the pre-charge circuitry consumes less power to drive the bit line from mid-level value to the full swing voltage. Hence, this cell behaves as an automatic bit line swing limiter and reduces the charge/discharge power of the read bit lines.

For the reduction of read power various techniques are there in literature that limits the voltage swing at the read bit line of which voltage swing limiter [10] and pulsed word line techniques [11] are the prominent ones. Both the techniques require extra hardware and accurate timing and control signals that make these techniques difficult to implement.

2) Strategy for Write Power Reduction

In the proposed 10T cell the differential voltage swing at the write bit lines is obtained by the read discharge instead of the write driver. The charge that is shared between the read and the write bit lines is used by the write bit lines to reduce power. The proposed 10T cell has a dedicated pair of write bit lines. So we don't need to use the pre-charge circuitry for the write bit lines. Instead a write driver is used that drives the bit lines high or low depending upon the data value. During read and hold cycles the bit lines remain floating and retain their charge. Again many scenarios are possible depending upon the data value written in two adjacent write cycles in the column.

Scenario1: Write '0' followed by a write '1' operation if the last written data was '0', the BL is low while BLB is high. The read discharge flows through the read path and M7to the BL during the read '0' cycle and charges the BL partially. If the next write cycle happens to be a write '1' cycle, the write driver has to drive the BL to high and BLB to low. But now, as the bit line BL is already at a mid level voltage, the write driver only has to drive it from mid level voltage to full swing voltage hence effectively reducing the write power.

Scenario2: Write '1' followed by a write '0' operation if the last written data was '1', the BLB is low while BL is high. The read discharge flows through the read path and M8 to the BLB during the read '0' cycle and charges the BLB partially. If the next write cycle happens to be a write '0' cycle, the write driver has to drive the BLB to high and BL to low. But now, as the bit line BLB is already at a mid level voltage, the write driver only has to drive it from mid level voltage to full swing voltage hence effectively reducing the write power.

Scenario3: Write '0' followed by a write '0'operation No write power benefits because already the bit lines are at their required voltages and no power is consumed. The charge gained by BLB is drained to ground.

Scenario4: Write '1' followed by a write '1' operation. Again no write power benefits because already the bit lines are at their required voltages and no power is consumed. The charge gained by BL is drained to ground.

Scenario5: Write '1' followed by write '0' when read '1' has taken place. During the read '1' operation read path is off but in this case BL is high and BLB is low. Hence the transistors M7 and M8 are ON and hence charge is shared between BL and BLB causing write power savings in the next write cycle.
All these write power gains are possible only after read '0' operation because during read '1' operation no active power is consumed that can be recycled.

3) Strategy for bit line leakage reduction

Addition of one transistor in the read path dramatically reduces the leakage in the read '1' mode.

Negative Bias Temperature Instability & Recovery Boosting

NBTI is a key reliability issue in MOSFETs. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and trans-conductance of a MOSFET. The degradation exhibits logarithmic dependence on time. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism also affects nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate.

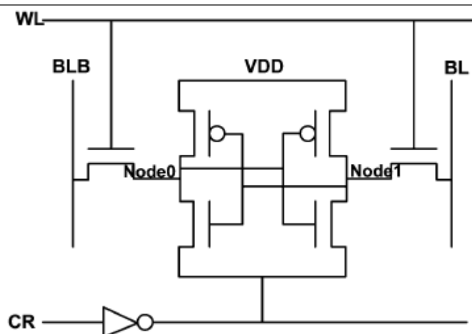

Figure 3: Modified SRAM Cell which Supports Recovery Boosting

Recovery Boosting: In the normal operating mode, the state of the bit lines change during read and writes operations. Since a pair of bit lines is shared by all the memory cells in a given column in the array, even those memory cells that are not being read from or written to will have the voltage on their bit lines changing. In an ordinary SRAM array, these bit line transitions do not affect the normal operation of the cells. However, in order to perform recovery boosting of a memory cell, both bit lines of the cell need to be raised to . Therefore, we need to be able to isolate the bit lines of the memory cells that are in the recovery boost mode from the bit lines that are used for accessing other cells in the array. To provide this isolation, we extend the memory cell with connections to the rail of an adjoining row or column via two pMOS access devices. The design of the modified SRAM cell is shown in Figure and an SRAM array that uses this cell for controlling individual entries to operate either in normal or recovery boost mode.

Schmitt Trigger Based SRAM Designs

In order to resolve the conflicting read versus write design requirements in the conventional 6T bit cell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in figure. During input transition, the feedback transistor (NF) tries to preserve the logic “1” at output ( ) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a input transition for the inverter storing logic “1,” higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bit cell. Two novel bit cell designs are proposed. The first ST-based SRAM bit cell has been presented in our earlier work. Another ST-based SRAM bit cell which further improves the bit cell stability has been reported in existing works. To maintain the clarity of the discussion, the ST bit cell in [30] is termed the “ST-1” bit cell while the other ST bit cell is termed the “ST-2” bit cell shown in the Figure below.

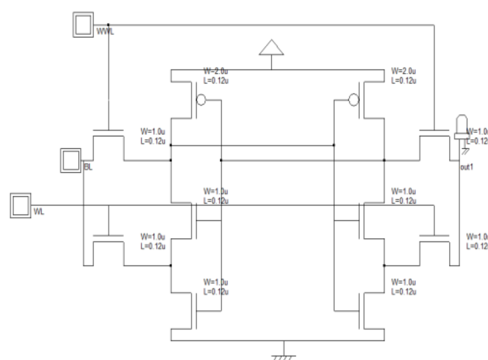

Figure 4: ST2 Bit Cell

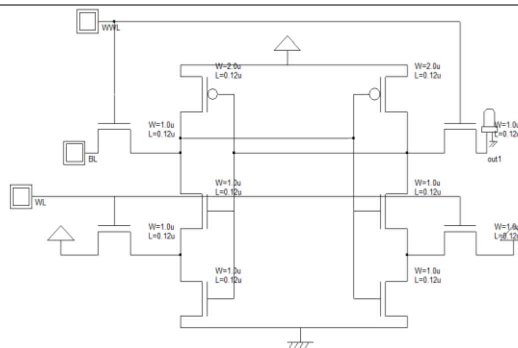

Figure 5: ST1 Bit Cell Proposed Low Power SRAM

As the Schmitt trigger based designs are having high number of transistor to make the read stability that is 10 Transistor which very high when compared to the existing 6T SRAM Design we are going to combine the mentioned read stability at the above part to our proposed work to reduce the count than the Schmitt trigger based designs at the same time we are going to achieve reduced power consumption with reduced transistor count without affecting the read stability. At the same time the proposed design supports separate read and write operations as in the Schmitt Trigger based designs. Our idea is to combine these two different technologies & to design a new circuit with much efficiency than the existing two designs. At the same time the proposed system is designed using minimal NBTI noise effects as we are combining the Recovery Boosting technology with our modified SRAM Design. The simulations show that there is a marginal improvement in Power consumption when compared to the existing designs. Here we are using high voltage transistors as which is designed to be switched ON at voltages above the normal acceptable limit and to dissipate the voltages above the normal limit to the ground. This design reduces the chances of Physical Damages in the circuit during voltage variations and at power fluctuation effects.

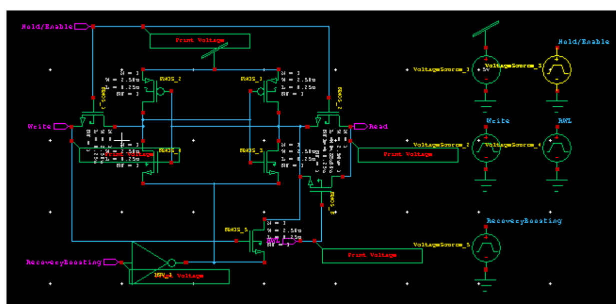

Figure 6: Proposed SRAM Cell with Recovery Boosting and High Voltage Transistors.

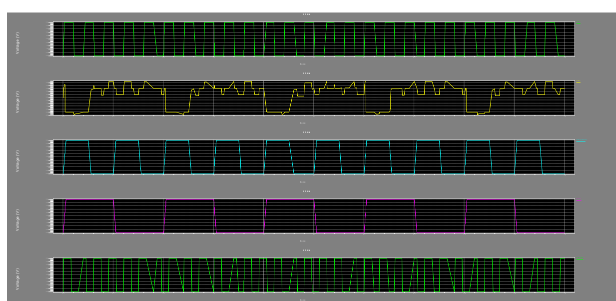

Figure 7: Power Analysis of Proposed Design

Tabulation & Results

Type	Power (Watts)
8T SRAM	**3.72 x 10^{-3}W**
10T SRAM	**1.89 x 10^{-3}W**
Proposed Method	**1.63 x10^{-3}W**

Conclusion

Our proposed design shows 67% that much less power than the existing ones which is 1.63mW at the standard TSMC018 Our Proposed layout combined with High Voltage Pass Transistor & Negative Bias Temperature Instability (NBTI) with read error reduction Circuit concept TSMC018 nano-meter technology. Thus this design can be used for future SRAM core memories. As both the problems are reduced we can able to reduce much more power which can be used for future low power memories.

Reference

[1]. Saumya Jain, K. Santhosh , Manisha Pattanaik , Balwinder Raj, “A 10-T SRAM cell with Inbuilt Charge Sharing for Dynamic Power Reduction” IEEE J. of Solid-State Circuits, 2013

[2]. International Technology Roadmap for Semiconductors 2011, http://www.itrs.net/Common/2011ITRS/Home2011.htm.

[3]. N.K. Shukla, S. Birla, M. pattanaik, “Speed and Leakage Power Tradeoff in Various SRAM Circuits,” International Journal of Computer and Electrical Engineering, Vol. 3, No. 2, April, 2011

[4]. J. Chang, D. Mohapatra, K. Roy, “A Priority-Based 6T/8T Hybrid SRAM Architecture for Aggressive Voltage Scaling in Video Applications,” IEEE Transactions On Circuits And Systems For Video Technology, Vol. 21, no. 2, pp.101-112, Feb. 2011.

[5]. N. Verma, A.P. Chandrakasan, "A 256 kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy," IEEE J. of Solid-State Circuits, vol.43, no.1, pp.141-149, Jan. 2008.

[6]. H. Noguchi, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, M. Yoshimoto, “ A 10T Non-Precharge Two-Port SRAM for 74% Power Reduction in Video Processing,” IEEE Computer Society Annual Symposium on VLSI, 2007 (ISVLSI '07).

[7]. C. H. Lo, S.Y. Huang, "P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation," IEEE Journal of Solid-State Circuits, vol.46, no.3, pp.695-704, March 2011.

[8]. K. Kim, H. Mahmoodi, K. Roy, "A Low-Power SRAM Using Bit-Line Charge-Recycling," IEEE J. of Solid-State Circuits, vol.43, no.2, pp.446- 459, Feb. 2008 .

[9]. J. Abella, X. Vera, and A. Gonzalez, “Penelope: The NBTI-aware processor,” in *Proc. 40th IEEE/ACM Int. Symp. Microarchitecture*, 2007.

[10]. H. Akkary, R. Rajwar, and S. T. Srinivasan, “Checkpoint processing and recovery: Towards scalable large instruction window processors,” in *Proc. Int. Symp. Microarchitecture (MICRO)*, Dec. 2003, pp. 423–434.

[11]. N. L. Binkert *et al.*, “The M5 simulator: Modeling networked systems,” *IEEE Micro*, vol. 26, no. 4, pp. 52–60, Jul. 2006.

[12]. P. Bose, J. Shin, and V. Zyuban, “Method for Extending Lifetime Reliability of Digital Logic Devices Through Removal of Aging Mechanisms,” U.S. Patent 7 489 161, Feb. 10, 2009.

[13]. A. Cabe, Z. Qi, S. Wooters, T. Blalock, and M. Stan, “Small embeddable NBTI sensors (SENS) for tracking on-chip performance decay,” in *Proc. Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2009, pp. 1–6.

[14]. O. Ergin, D. Balkan, D. Ponomarev, and K. Ghose, “Increasing processor performance through early register release,” in *Proc. Int. Conf. Comput. Design (ICCD)*, Oct. 2004, pp. 480–487.